Single-Stage PFC Controller **SG6980**

FEATURES OVERVIEW

- Innovative switching-charge multiplier divider
- Multi-vector control for improved PFC output transient response
- 1:1 Synchronous switching with SYNC
- Average current mode control
- Remote on/off control
- Power-on sequence control
- Programmable PFC output-voltage control
- Cycle-by-cycle current limiting
- Over-voltage and under-voltage protections
- Brownout and open-loop protections
- Low start-up and operating current

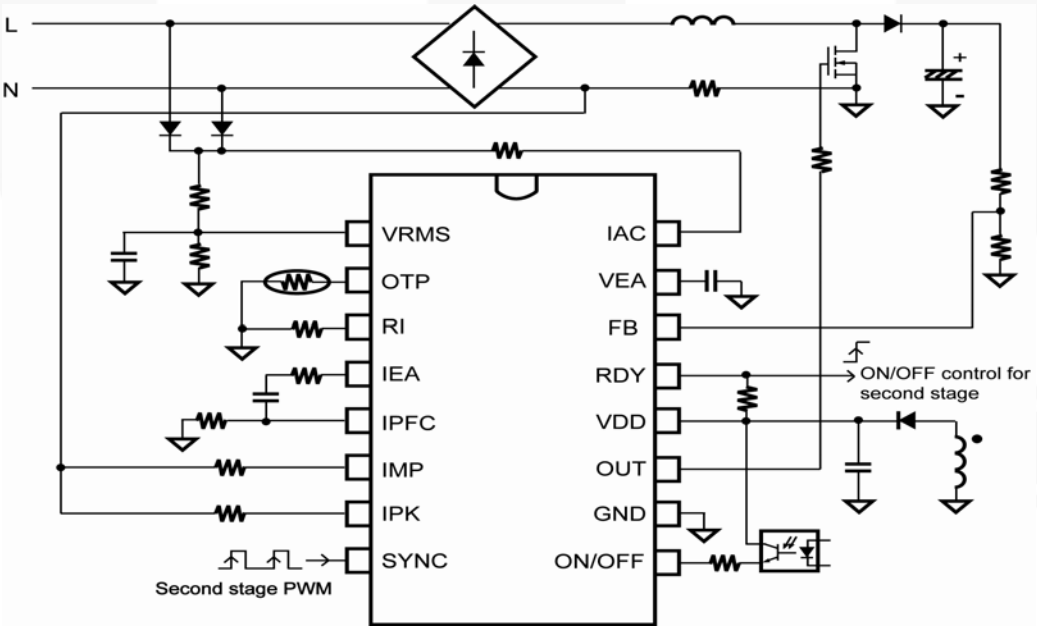
APPLICATIONS

- Active-PFC switching power supplies
- TV and home appliances
- Computer and telecom

DESCRIPTION

The highly integrated SG6980 is designed for power supplies with boost power-factor-correction (PFC). It requires very few external components to achieve desirable operation and includes versatile protections / compensation. It is available in 16-pin DIP and SOP packages. The innovative switching-charge multiplier divider enhances the PFC circuit's noise immunity. The proprietary multi-vector control scheme provides a fast transient response in a low-bandwidth PFC loop, in which the overshoot and undershoot of the PFC voltage are clamped. If the feedback loop is broken, SG6980 shuts off to prevent extra-high voltage on output. The PFC gate driver can be synchronized with external SYNC signal and the switching noise can be reduced. During start-up, the RDY (ready) is pulled low until the PFC output voltage reaches the setting level. This signal can be used to control the second forward stage for proper power-on sequence. In addition, SG6980 provides complete protection functions, such as brownout and RI open/short.

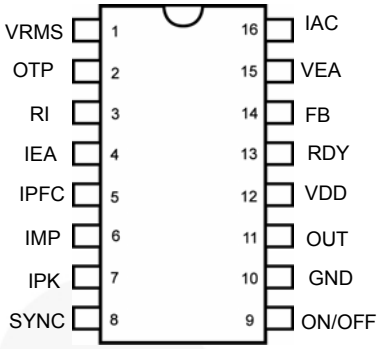
TYPICAL APPLICATION



MARKING DIAGRAMS

T: D = DIP S=SOP
P: Z = Lead Free
XXXXXXXX: Wafer Lot
Y: Year; WW: Week
V: Assembly Location

PIN CONFIGURATION



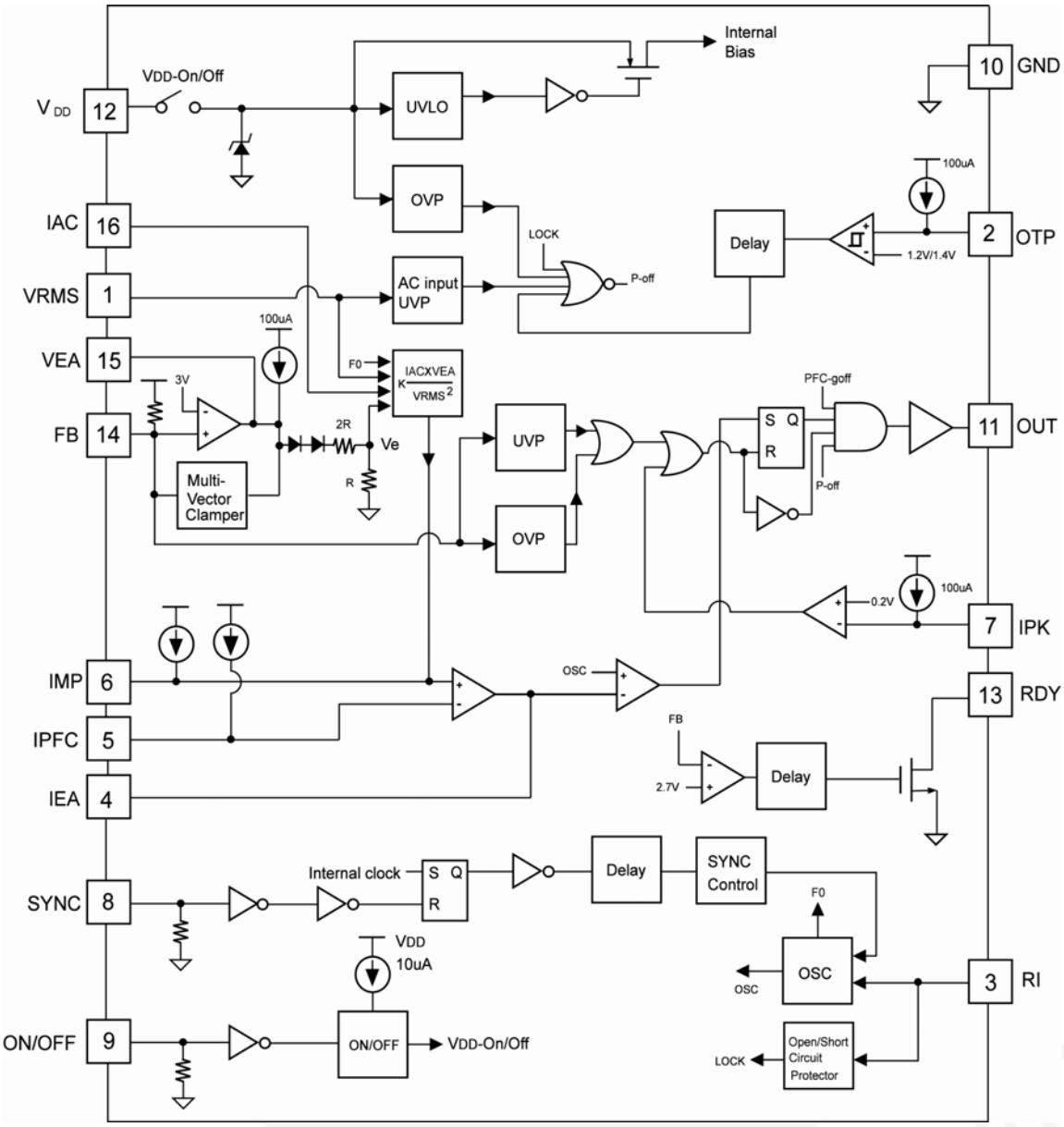
ORDERING INFORMATION

Part Number	Pb-Free	Package
SG6980DZ		16-Pin DIP
SG6980SZ		16-Pin SOP

PIN DESCRIPTIONS

Name	Pin	Type	Function
VRMS	1	Line-Voltage Detection	Line voltage detection. The pin is used for PFC multiplier and brownout protection. For brownout protection, the controller is disabled with a 195ms delay time when the VRMS voltage drops below 0.8V. There is a 200mV hysteresis for brownout protection.
OTP	2	Over-Temperature Protection	This pin supplies an over-temperature protection signal. A constant current is output from this pin. If RI is equal to 24kΩ, the magnitude of the constant current is 50μA. An external NTC thermistor must be connected from this pin to ground. The impedance of the NTC thermistor decreases whenever the temperature increases. Once the voltage of the OTP pin drops below 1.2V, the SG6980 is off, and auto restarts when the voltage is back to 1.4V.
RI	3	Oscillator Setting	The resistance of a resistor connected between RI and ground determines the switching frequency. A resistance between 15kΩ and 40KΩ is recommended. The switching frequency is equal to [1560 / RI] kHz, where RI is in kΩ. For example, if RI is equal to 24kΩ, then the switching frequency is 65kHz.
IEA	4	Current Amplifier Output	This is the output of the PFC current amplifier. The signal from this pin is compared with an internal sawtooth and determines the pulse width for PFC gate drive.
IPFC	5	Inverting Input for PFC Current Amplifier	The inverting input of the PFC current amplifier. Proper external compensation circuits will result in excellent input power factor via average-current-mode control.
IMP	6	Non-inverting Input for PFC Current Amplifier and Output of Multiplier	The non-inverting input of the PFC current amplifier and also the output of the multiplier. Proper external compensation circuits result in excellent input power factor via average-current-mode control.
IPK	7	Peak Current Limit	The peak current setting for PFC.
SYNC	8	Synchronous Signal	This pin receives the external switching signal. The PFC switching can be synchronized by SYNC with 1:1 ratio.
ON/OFF	9	Remote On/Off	Active high. The SG6980 is disabled whenever the voltage at this pin is lower than 1V or the pin is open. When SG6980 is disabled by ON/OFF, the I_{DD} current is lower than 35μA.
GND	10	Ground	The ground.
OUT	11	Gate Drive	The totem pole output drive for the PFC MOSFET. This pin is internally clamped under 18V to protect the MOSFET.
VDD	12	Supply	The power supply pin. The threshold voltages for start-up and turn-off are 12.5V and 10V, respectively. The operating current is lower than 5mA.
RDY	13	Ready Signal Output	This pin outputs a ready signal to control the power on sequence. Once the SG6980 is turned on and the FB (PFC feedback input) voltage is higher than 2.7V, this pin locks high impedance. Disabling the SG6980 resets this pin to the low.
FB	14	Feedback Input	The feedback input for PFC voltage loop. The inverting input of PFC error amplifier. This pin is connected to the PFC output through a divider network.
VEA	15	Error Amplifier Output	The error amplifier output for PFC voltage feedback loop. A compensation network (usually a capacitor) is connected between this pin and ground. A large capacitor value results in a narrow bandwidth and improves the power factor.
IAC	16	Input AC Current	This input is used to provide current reference for the multiplier. The suggested maximum I_{AC} is 350μA.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATING

Symbol	Parameter	Value		Unit
V_{VDD}	DC Supply Voltage*	25		V
I_{AC}	Input AC Current	2		mA
V_{High}	OUT, SYNC, ON/OFF, RDY	-0.3 to 25V		V
V_{Low}	Others	-0.3 to 7V		V
P_D	Power Dissipation	DIP	0.8	W
		SOP	0.4	
T_J	Operating Junction Temperature	+150		℃
T_A	Operating Ambient Temperature Range	-20~+125		
T_{STG}	Storage Temperature RDY	-55 to +150		℃
$R_{\theta j\text{-}C}$	Thermal resistance (Junction-to-Case)	DIP	36.70	℃/W
		SOP	37.76	
T_L	Lead Temperature (Wave Soldering or IR, 10 Seconds)	260		℃
$V_{ESD,HBM}$	ESD Capability, Human Body Model	4		KV
$V_{ESD,MM}$	ESD Capability, Machine Model	250		V

*All voltage values, except differential voltages, are given with respect to the network ground terminal.

*Stress beyond those listed under "ABSOLUTE MAXIMUM RATING" may cause permanent damage to the device.

ELECTRICAL CHARACTERISTICS

V_{DD}=15V, T_A=25°C unless otherwise noted.

V_{DD} Section

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{DD\text{-}OP}$	Continuously Operating Voltage				20	V
$I_{DD\text{-}OP}$	Operating Current	RI= 24KΩ,V_{DD} = 15V; Gate Open		4	5	mA
$I_{IC\text{-}OFF}$	Input Current	$V_{ON/OFF}$<V_{ON} , V_{DD}=25V		25	35	μA
$I_{DD\text{-}ST}$	Start-up Current	V_{DD}＜$V_{DD\text{-}ON}$-0.16V		10	20	μA
$V_{DD\text{-}ON}$	Start Threshold Voltage		11.5	12.5	13.5	V
$V_{DD\text{-}OFF}$	Minimum Operating Voltage		9	10	11	V
$V_{DD\text{-}OVP}$	V_{DD} Over-Voltage Protection with a Debounce Time		23.5	24.5	25.5	V
$t_{D\text{-}VDDOVP}$	Debounce Time of V_{DD} OVP		10		40	μs

Oscillator & Green-Mode Operation

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
F_{OSC}	PWM Frequency	RI= 24KΩ	62	65	68	KHz
RI	Nominal RI Value		15		40	KΩ
RI_{OPEN}	Maximum RI Value for Protection			200		KΩ
RI_{SHORT}	Maximum RI Value for Protection			2		KΩ

V_{RMS} for UVP and RDY

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{RMS-UVP-1}$	RMS AC Voltage Under-Voltage Threshold (with T_{UVP} Delay)		0.75	0.80	0.85	V
$V_{RMS-UVP-2}$	Recovery Level on VRMS for UVP Mode		$V_{RMS-UVP-1}$ +0.18	$V_{RMS-UVP-1}$ +0.20	$V_{RMS-UVP-1}$ +0.22	V
t_{UVP}	Under-Voltage Protection Propagation Delay Time (No Delay at Start-up)		150	195	240	ms

Voltage Error Amplifier

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{REF}	Reference Voltage		2.95	3	3.05	V
Av	Open-Loop Gain			60		dB
Z_o	Output Impedance			110		KΩ
OVP_{FB}	PFC Over-Voltage Protection on FB		1.066 • V_{REF}	1.083 • V_{REF}	1.100 • V_{REF}	V
$\triangle OVP_{FB}$	PFC Feedback Voltage Protection Hysteresis		60	90	120	mV
$t_{OVP-PFC}$	Debounce Time of PFC OVP		40	70	120	μs
V_{FB-H}	Clamp-High Feedback Voltage		1.033 • V_{REF}	1.050 • V_{REF}	1.066 • V_{REF}	V
G_{FB-H}	Clamp-High Gain			500		μA/mV
V_{FB-L}	Clamp-Low Feedback Voltage		0.916 • V_{REF}	0.950 • V_{REF}	0.966 • V_{REF}	V
G_{FB-L}	Clamp-Low Gain			6.5		μA/mV
I_{FB-L}	Clamp-Low Maximum Current		1.5	2		mA
UVP_{FB}	PFC Feedback Under-Voltage Protection		0.35	0.40	0.45	V
$t_{UVP-PFC}$	Debounce Time of PFC Feedback UVP		40	70	120	μs

Current Error Amplifier

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_{OFFSET}	Input Offset Voltage ((-) > (+))			8		mV
A_I	Open-Loop Gain			60		dB
BW	Unit Gain Bandwidth			1.5		MHz
CMRR	Common-Mode Rejection Ratio	V_{CM} = 0 ~ 1.5V		70		dB
$V_{OUT-HIGH}$	Output High Voltage		3.2			V
$V_{OUT-LOW}$	Output Low Voltage				0.2	V
I_{MR1}, I_{MR2}	Reference Current source	RI=24KΩ (I_{MR}=20+I_{RI} • 0.8)	50		70	μA
I_L	Maximum Source Current		3			mA
I_H	Maximum Sink Current			0.25		mA

Peak Current Limit

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_P	Constant Current Output	RI = 24KΩ	90	100	110	μA
V_{PK}	Peak Current Limit Threshold Voltage Cycle-by-Cycle Limit (V_{sense} < V_{pk})	V_{RMS}=1.05V	0.15	0.20	0.25	V
		V_{RMS}=3V	0.35	0.40	0.45	V
t_{PD-PFC}	Propagation Delay				200	ns
$t_{LEB-PFC}$	Leading-Edge Blanking Time		250	330	430	ns

Multiplier

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{AC}	Input AC Current	Linear RDY	0		360	μA
I_{MO-MAX}	Maximum Multiplier Current Output	RI=24 KΩ	230	250		μA
I_{MO-1}	Multiplier Current Output (Low-Line, High-Power)	V_{RMS}=1.05V; I_{AC}=90μA; V_{EA}=7.5V; RI=24KΩ	200	250	280	μA
I_{MO-2}	Multiplier Current Output (High-Line, High-Power)	V_{RMS}=3V; I_{AC}=264μA; V_{EA}=7.5V; RI=24KΩ	65	85		μA
V_{IMP}	Voltage of IMP Open		3.4	3.9	4.4	V

PFC Output Driver

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
V_Z	Output Voltage Maximum (clamp)	V_{DD}=20V		15	18	V
V_{OL}	Output Voltage Low	V_{DD} = 15V; I_O = 100mA			1.5	V
V_{OH}	Output Voltage High	V_{DD} = 13V; I_O = 100mA	8			V
t_R	Rising Time	V_{DD} = 15V; C_L = 5nF; OUT = 2V to 9V	30	70	120	ns
t_F	Falling Time	V_{DD} = 15V; C_L = 5nF; OUT = 9V to 2V	30	50	100	ns
DCY_{MAX}	Maximum Duty Cycle		93		98	%

RDY Section

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$FB_{RDY-high}$	FB Voltage, RDY High Impedance			2.7		V
$I_{FB-RDY-high}$	Input Leakage Current, RDY High Impedance	FB=2.5V			500	nA
V_{OL}	Output Voltage Low, RDY Failed	I_{SINK} =1mA			0.5	V
$t_{RDY-delay\ time}$	Interval Between FB > 2.7V and RDY High Impedance			4	6	ms
$t_{RDY-UVP_delay\ time}$	Delay Time Between Gate off and RDY Pull Low when UVP Occurs		10		16	ms

OTP Section

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
I_{OTP}	OTP Pin Output Current	RI = 24KΩ	90	100	110	μA
$V_{OTP-OFF}$	OTP Threshold Voltage		1.15	1.20	1.25	V
V_{OTP-ON}	Recovery Level on OTP		1.35	1.40	1.45	V
T_{OTP}	OTP Debounce Time		10		40	μs

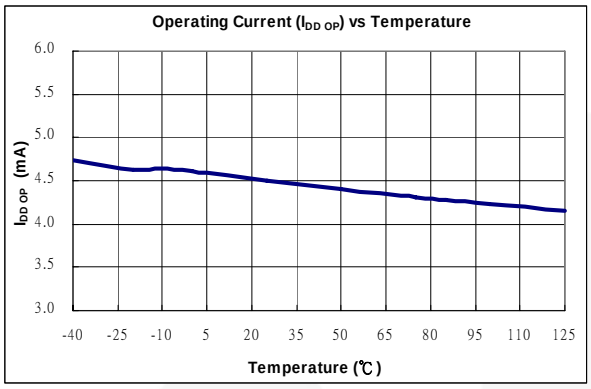
SYNC Section

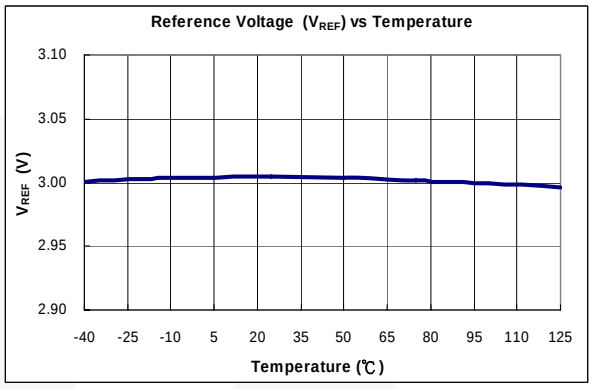
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$V_{SYNC-HIGH}$	Synchronizing Signal High Threshold		3.5			V
$V_{SYNC-LOW}$	Synchronizing Signal Low Threshold				0.9	V
F_{Min}	Minimum Synchronizing Frequency	RI=24KΩ	F_{OSC}-6			KHz
F_{Max}	Maximum Synchronizing Frequency				150	KHz
$t_{MIN_PULSE_W}$	Minimum Synchronizing Pulse Width	RI = 24KΩ	100	200	500	ns
$t_{MAX_PULSE_W}$	Maximum Synchronizing Pulse Width	RI = 24KΩ		15.8		µs
$t_{D-65KHZ}$	Delay Time Between SYNC and OUT, Switching Frequency = 65KHz	RI=24KΩ	1		3	µs
$t_{D-50KHZ}$	Delay Time Between SYNC and OUT, Switching Frequency = 50KHz	RI=31.2KΩ	1		3	µs

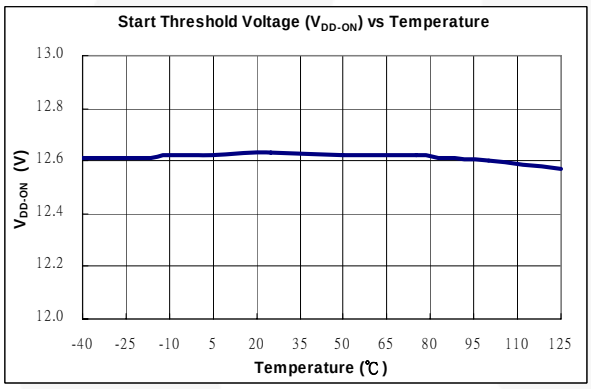
ON/OFF Section

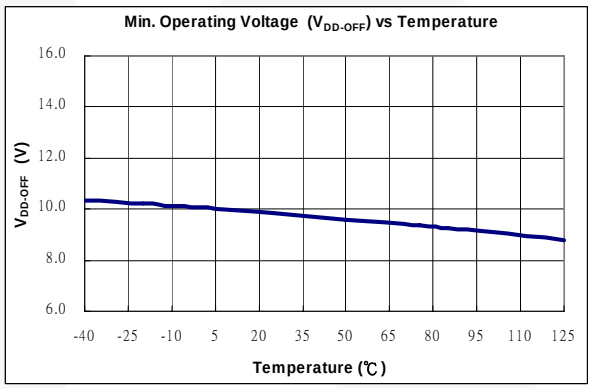
Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
$R_{on/off}$	Impedance of ON/OFF Pin		18	27	50	KΩ
V_{ON}	Enable Signal High Threshold		3			V
V_{OFF}	Enable Signal Low Threshold				1	V

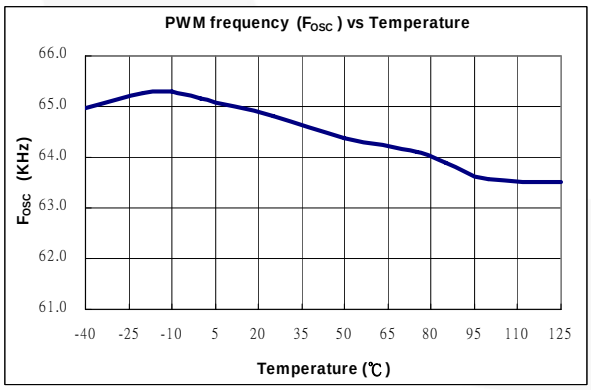
TYPICAL CHARACTERISTICS

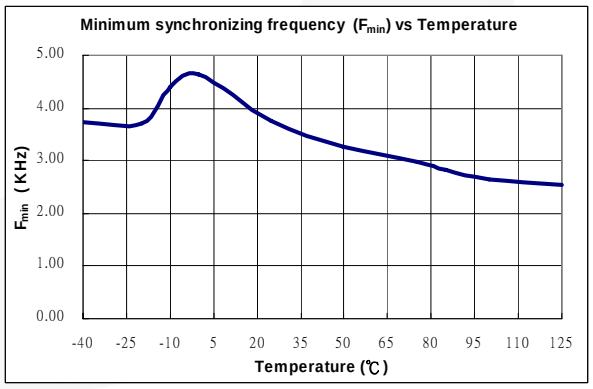


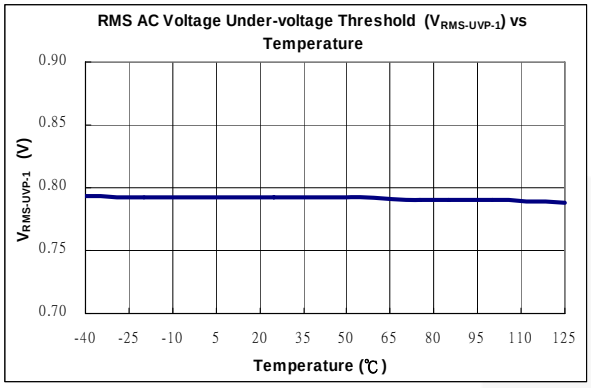


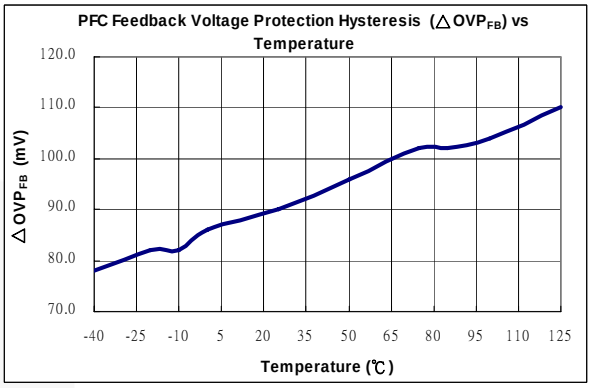


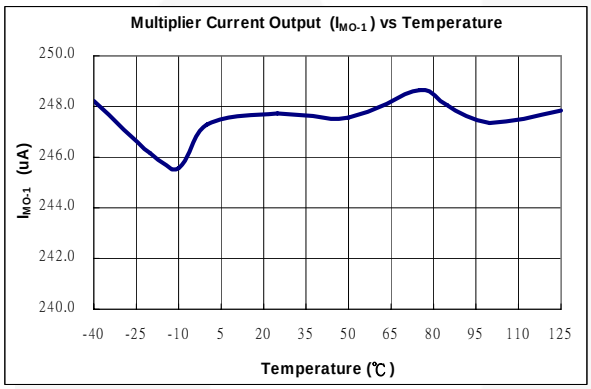


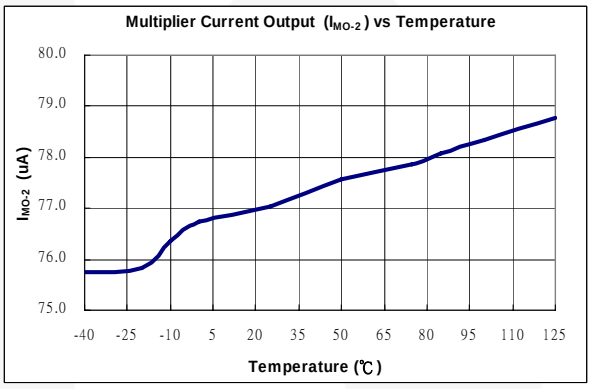


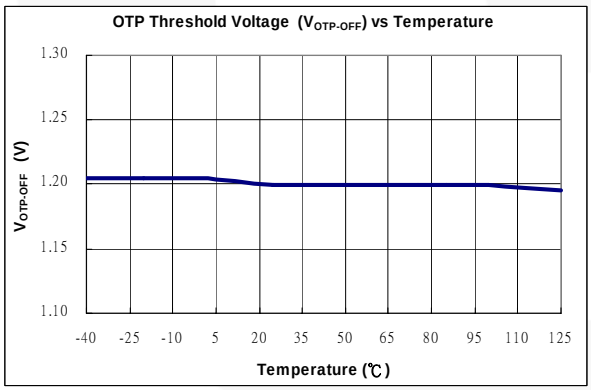


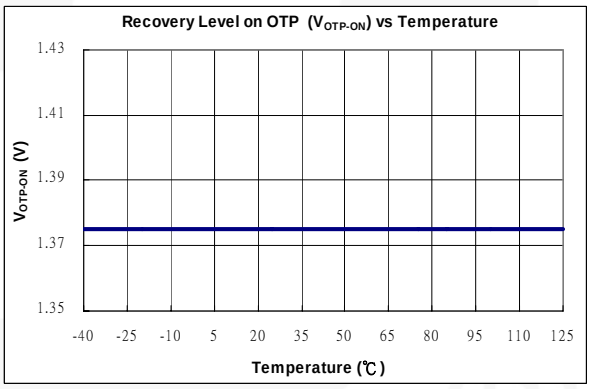

RMS AC Voltage Under-voltage Threshold ($V_{RMS-UVP-1}$) vs Temperature
$V_{RMS-UVP-1}$ (V)
0.90
0.85
0.80
0.75
0.70
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (℃)


PFC Feedback Voltage Protection Hysteresis ($\triangle OVP_{FB}$) vs Temperature
$\triangle OVP_{FB}$ (mV)
120.0
110.0
100.0
90.0
80.0
70.0
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (℃)


Multiplier Current Output (I_{MO-1}) vs Temperature
I_{MO-1} (uA)
250.0
248.0
246.0
244.0
242.0
240.0
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (℃)


Multiplier Current Output (I_{MO-2}) vs Temperature
I_{MO-2} (uA)
80.0
79.0
78.0
77.0
76.0
75.0
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (℃)


OTP Threshold Voltage ($V_{OTP-OFF}$) vs Temperature
$V_{OTP-OFF}$ (V)
1.30
1.25
1.20
1.15
1.10
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (℃)


Recovery Level on OTP (V_{OTP-ON}) vs Temperature
V_{OTP-ON} (V)
1.43
1.41
1.39
1.37
1.35
-40 -25 -10 5 20 35 50 65 80 95 110 125
Temperature (℃)

OPERATION DESCRIPTION

The highly integrated SG6980 is designed for a power supply with boost PFC. It requires very few external components to achieve high performance and includes versatile protections / compensation.

The PFC function is implemented by average current mode control. The patented switching-charge multiplier-divider provides a high-degree of noise immunity for the PFC circuit. This enables the PFC circuit to operate over a much wider region. The proprietary multi-vector output voltage control scheme provides a fast transient response in a low-bandwidth PFC loop, in which the overshoot and undershoot of the PFC voltage are clamped. If the feedback loop is broken, the SG6980 shuts off PFC to prevent extra-high voltage on output. Programmable two-level high/low line compensation optimizes THD performance.

In addition, SG6980 provides complete protection functions, such as brownout and RI open/short.

Switching Frequency and Current Sources

The switching frequency of SG6980 can be programmed by the resistor R_I connected between RI pin and GND. The relationship is:

$$f_{PWM} = \frac{1560}{R_I\ (k\Omega)}(kHz) \text{ ----------} \quad (1)$$

For example, a 24kΩ resistor R_I results in a 65kHz switching frequency. Accordingly, constant current I_T flows through R_I.

$$I_T = \frac{1.2V}{R_I\ (k\Omega)}(mA) \text{ ----------} \quad (2)$$

I_T is used to generate internal current reference.

If there is a SYNC signal input, the switching frequency is defined by the SYNC signal. The SNYC frequency must be larger than the programmed switching frequency, less 6KHz.

Line Voltage Detection (V_{RMS})

Figure 1 shows a resistive divider with low-pass filtering for line-voltage detection on the VRMS pin. The V_{RMS} voltage is used for the PFC multiplier, brownout protection, and RDY control.

For brownout protection, the SG6980 is disabled with 195ms delay time if the voltage V_{RMS} drops below 0.8V.

For PFC multiplier and RDY control, please refer to below sections for more detail.

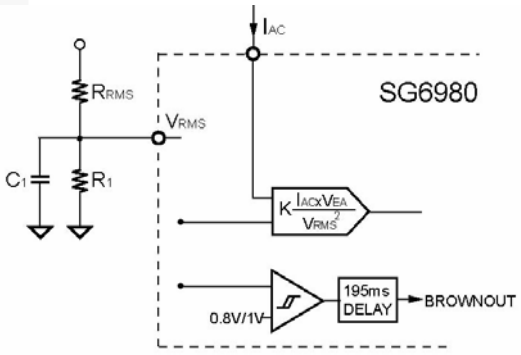


FIG.1

PFC Output Voltage Control

For a universal input (90VAC ~ 264VAC) power supply applying active boost PFC and forward as a second stage, the output voltage of PFC is usually designed around 400V.

$$Vo = \frac{R_A + R_B}{R_B} \times 3V \text{ ----} \quad (3)$$

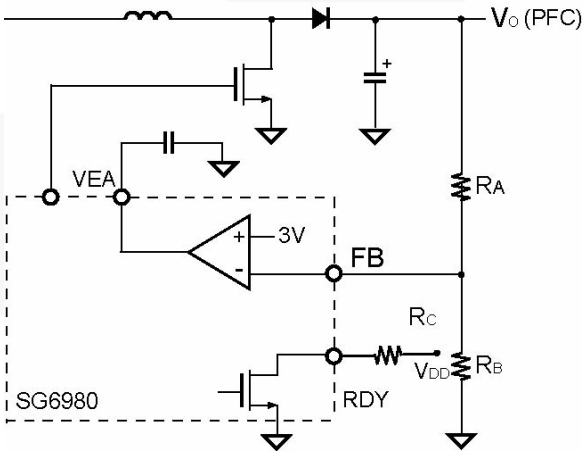


FIG.2 Output Voltage Setting

ON/OFF

For ON/OFF control, the SG6980 is disabled immediately if the voltage at this pin is below 1V. Usually, the pin opens when turn off can have the best power saving. The operating current during turn off is less than 35µA.

SYNC Signal Section

The SG6980 can synchronize the OUT and synchronize signals provided by second stage, which reduces switching noise and the ripple on output voltage. Figure 3 shows the relationship between the OUT and SYNC signals.

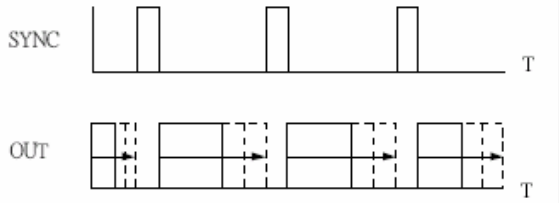


FIG.3 Synchronized Interleaving-Switching

RDY Signal Section

SG6980 provides a RDY pin to inform the next stage and other applications. RDY signal is high impedance when the FB voltage goes up to 2.7V and delays around 5ms. Use the pin to turn on the second stage PWM when the bulk capacitor voltage is high enough. In SG6980, the RDY pin (open-drain structure) is used for next-stage-ready signal.

PFC Operation

The purpose of a boost active power factor corrector (PFC) is to shape the input current of a power supply. The input current waveform and phase follow that of the input voltage. Using SG6980, average-current-mode control is utilized for continuous-current-mode operation for the PFC booster. With the innovative multi-vector control for voltage loop and switching-charge multiplier/divider for current reference, excellent input power factor is achieved with good noise immunity and transient response. Figure 4 shows the total control loop for the average-current-mode control circuit of SG6980.

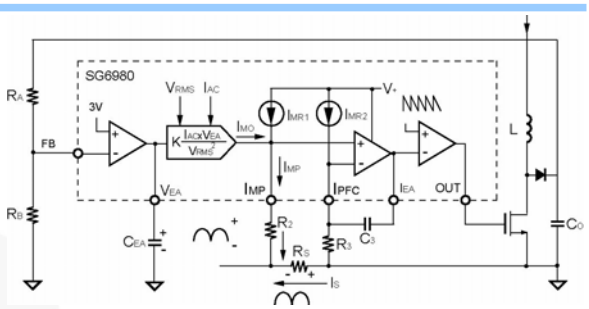


FIG.4 Multiplier and Control Loop of PFC Stage

The current source output from the switching-charge multiplier/divider can be expressed as:

$$I_{MO} = K \times \frac{I_{AC} \times V_{EA}}{V_{RMS}^2} (\mu A) \quad \text{----------} \quad (4)$$

I_{MP}, the current output from IMP pin, is the summation of I_{MO} and I_{MR1}. I_{MR1} and I_{MR2} are identical, fixed-current sources. R_2 and R_3 are also identical. They are used to pull high the operating point of the IMP and ICS pins if the voltage across R_S goes negative with respect to ground.

Through the differential amplification of the signal across Rs, better noise immunity is achieved. The output of IEA is compared with an internal sawtooth and the pulse width for PFC is determined. Through the average current-mode control loop, the input current I_S is proportional to I_{MO}:

$$I_{MO} \times R_2 = I_S \times R_S \quad \text{----------} \quad (5)$$

According to Equation 5, the minimum value of R_2 and maximum of R_S can be determined because I_{MO} should not exceed the specified maximum value.

There are different concerns in determining the value of the sense resistor, R_S. The value of R_S should be small enough to reduce power consumption, large enough to maintain the resolution. A current transformer (CT) may be used to improve the efficiency of high-power converters.

To achieve a good power factor, the voltage for V_{RMS} and V_{EA} should be kept as DC as possible, according to Equation 4. Good RC filtering for V_{RMS} and narrow bandwidth (lower than the line frequency) for voltage loop are suggested for better input current shaping. The transconductance error amplifier has output impedance R_O and a capacitor C_{EA} (1µF ~ 10µF) connected to ground (as shown in Figure 4). This establishes a dominant pole *f1* (per Equation 6) for the voltage loop.

$$f_1 = \frac{1}{2\pi \times R_0 \times C_{EA}} \quad \text{----------} \quad (6)$$

The average total input power can be expressed as:

$$\begin{aligned} Pin &= Vin(rms) \times Iin(rms) \\ &\propto V_{RMS} \times I_{MO} \\ &\propto V_{RMS} \times \frac{I_{AC} \times V_{EA}}{V_{RMS}^2} \\ &\propto V_{RMS} \times \frac{\frac{Vin}{R_{AC}} \times V_{EA}}{V_{RMS}^2} \propto V_{EA} \end{aligned} \quad \text{----------} \quad (7)$$

From Equation 7, V_{EA}, the output of the voltage error amplifier, controls the total input power and the power delivered to the load.

Multi-Vector Error Amplifier

The voltage-loop error amplifier of SG6980 is transconductance, which has high output impedance (> 90kΩ). A capacitor C_{EA} (1μF ~ 10μF) connected from VEA to ground provides a dominant pole for the voltage loop. Although the PFC stage has a low bandwidth voltage loop for better input power factor, the innovative multi-vector error amplifier provides a fast transient response to clamp the overshoot and undershoot of the PFC output voltage. Figure 5 shows the voltage loop with multi-vector for fast transient error amplifier. When the variation of the feedback voltage exceeds ± 5% of the reference voltage, the transconductance error amplifier adjusts its output impedance to increase the loop response. If the feedback resistance is opened, SG6980 shuts off immediately to prevent extra-high voltage on the output capacitor.

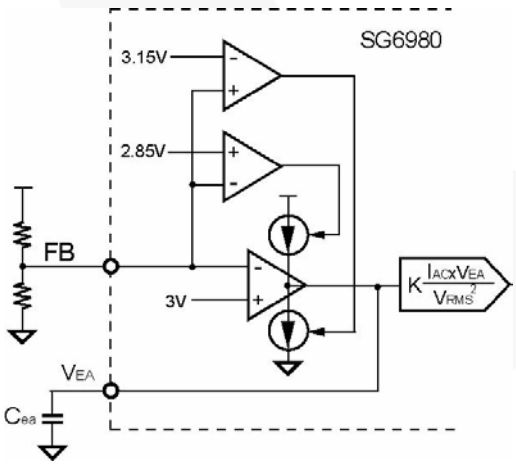


FIG. 5 Voltage Error Amplifier with Multi-Vector

Cycle-by-Cycle Current Limiting

SG6980 provides cycle-by-cycle current limiting for PFC stages. Figure 6 shows the peak current limit for the PFC stage. The PFC gate drive is terminated once the voltage on IPK pin goes below V_{PK}.

The voltage of V_{RMS} determines the voltage of V_{PK}. The relationship between V_{PK} and V_{RMS} is shown in Figure 6.

The amplitude of the constant current I_P is determined by the internal current reference I_T, according to the equation:

$$Ip = 2 \times I_T = 2 \times \frac{1.2V}{R_I} \quad \text{----------} \quad (8)$$

Therefore the peak current of the I_S is given by:

$$Is_peak = \frac{(Ip \times R_P) - V_{pk}}{R_S} \quad \text{----------} \quad (9)$$

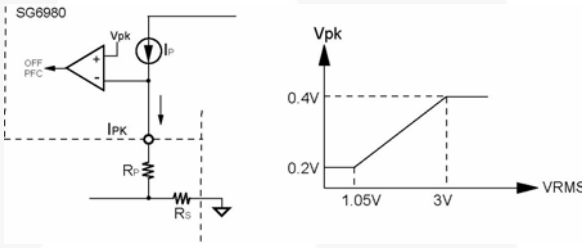


FIG.6 Current Limit

Gate Drivers

SG6980 output stages are fast totem-pole gate drivers. The output driver is clamped by an internal 18V Zener diode to protect the power MOSFET.

Over-Temperature Protection

SG6980 provides an OTP pin for over-temperature protection. A constant current is output from this pin. If RI is equal to 24kΩ, the magnitude of the constant current is 50μA. An external NTC thermistor must be connected from this pin to ground. When the OTP voltage drops below 1.2V, SG6980 shuts down. SG6980 auto restarts when the OTP voltage is higher than 1.4V.

Protections & Built-in Latch Circuit

The SG6980 provides full protection functions to prevent the power supply and the load from being damaged. The protection features include:

PFC Feedback Over-Voltage Protection. When the PFC feedback voltage exceeds the over-voltage threshold, the SG6980 inhibits the PFC switching signal. This protection prevents the PFC power converter from operating abnormally while the FB pin is open.

PFC Feedback Under-Voltage Protection. The SG6980 stops the PFC switching signal whenever the PFC feedback voltage drops below the under-voltage threshold. This protection feature is designed to prevent the PFC power converter from experiencing abnormal conditions while the FB pin is shorted to ground.

VDD Over-Voltage Protection. The built-in clamping circuit clamps V_{DD} whenever the V_{DD} voltage exceeds the over-voltage threshold.

RI Pin Open / Short Protection. The RI pin is used to set the switching frequency and internal current reference. If the RI pin is short or open, SG6980 is off.

PCB Layout

SG6980 has a single ground pin. High sink currents in the output therefore cannot be returned separately. Good high-frequency or RF layout practices should be followed. Avoid long PCB traces and component leads. Locate decoupling capacitors near the SG6980. A resistor of 5 ~ 20Ω is recommended, connecting in series from the output to the gate of the MOSFET.

Isolating the interference between the PFC and PWM stages is also important. Figure 7 shows an example of the PCB layout. The *ground trace 1* is connected from the ground pin to the decoupling capacitor, which should be low impedance and as short as possible. The *ground trace 2* provides a signal ground. It should be connected directly to the decoupling capacitor C_{DD} and/or to the ground pin. The *ground trace 3* is independently tied from the decoupling capacitor to the PFC output capacitor C_O. The ground in the output capacitor C_O is the major ground reference for power switching. To provide a good ground reference and reduce the switching noise of both the PFC and PWM stages, the *ground traces 6 and 7* should be located very near and be low impedance.

The ICS pin is connected directly to R_S through R_3 to improve noise immunity. (Beware that it may incorrectly be connected to the ground trace 2). The IMP and IPK pins should also be connected directly, via the resistors R_2 and R_P, to another terminal of R_S.

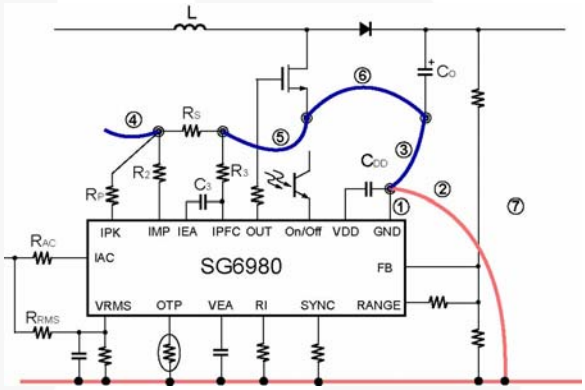
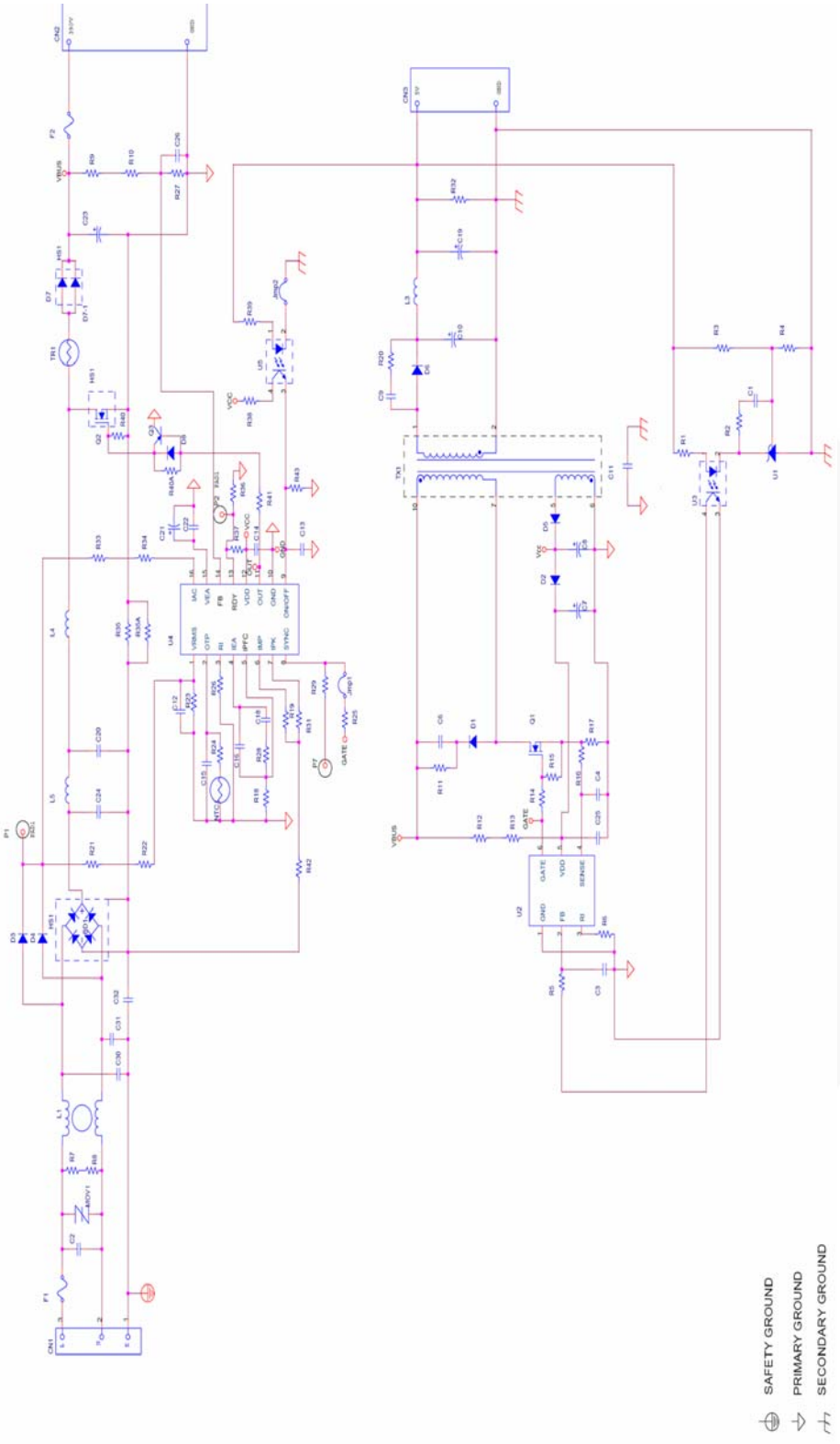


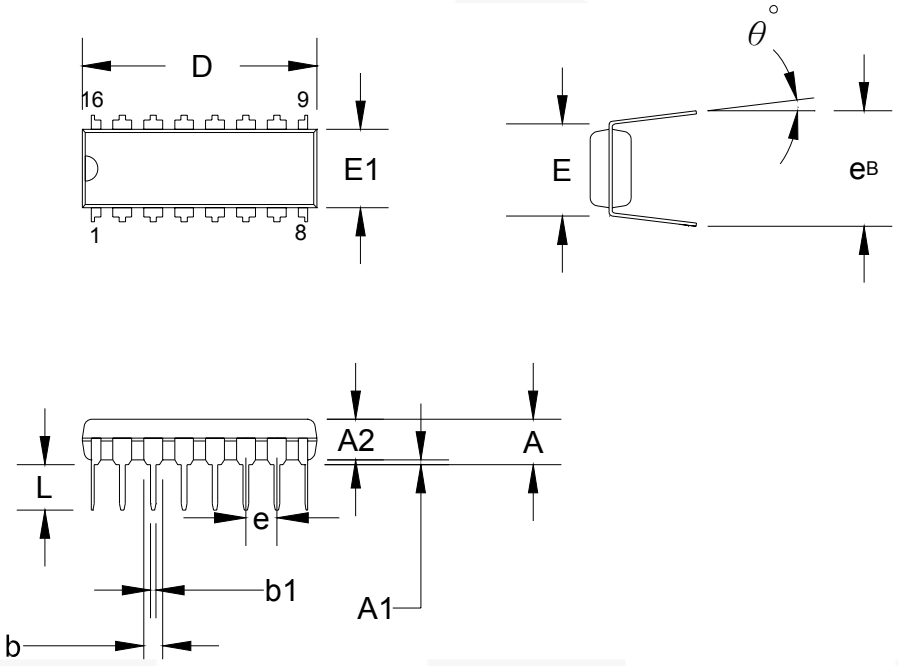
FIG. 7 PCB Layout

REFERENCE CIRCUIT



PACKAGE INFORMATION

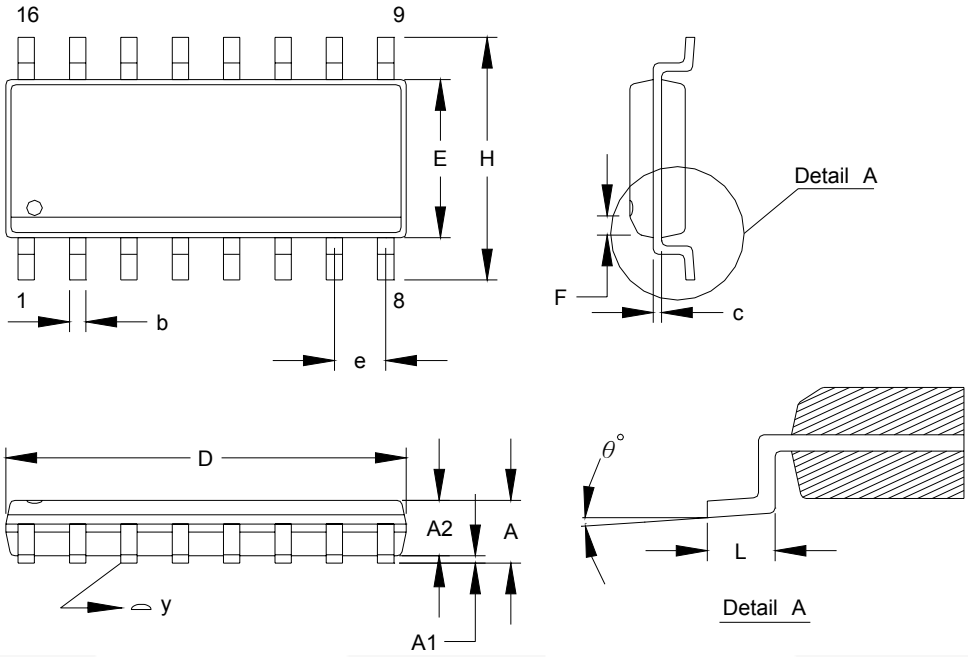
16 PINS – PLASTIC DIP (D)



Dimensions:

Symbol	Millimeter			Inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A			5.334			0.210
A1	0.381			0.015		
A2	3.175	3.302	3.429	0.125	0.130	0.135
b		1.524			0.060	
b1		0.457			0.018	
D	18.669	19.177	19.685	0.735	0.755	0.775
E		7.620			0.300	
E1	6.121	6.299	6.477	0.241	0.248	0.255
e		2.540			0.100	
L	2.921	3.302	3.810	0.115	0.130	0.150
e_B	8.509	9.017	9.525	0.335	0.355	0.375
θ°	0°	7°	15°	0°	7°	15°

16 PINS – PLASTIC SOP (S)



Dimension:

Symbol	Millimeter			Inch		
	Min.	Typ.	Max.	Min.	Typ.	Max.
A	1.346		1.753	0.053		0.069
A1	0.101		0.254	0.004		0.010
A2	1.244		1.499	0.049		0.059
b		0.406			0.016	
c		0.203			0.008	
D	9.804		10.008	0.386		0.394
E	3.810		3.988	0.150		0.157
e		1.270			0.050	
H	5.791		6.198	0.228		0.244
L	0.406		1.270	0.016		0.050
F		0.381X45°			0.015X45°	
y			0.101			0.004
θ°	0°		8°	0°		8°

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2. A critical component in any component of a life support, device, or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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